

Sheet 3 of 12

Form 1449*

Atty. Docket No.: 303.389US2

Serial No. Unknown

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

Applicant: Leonard Forbes et al.

Filing Date: Herewith

Group: Unknown

U.S. PATENT DO	CUMENTS
----------------	---------

*Examiner Initial	Document Mumber	Data	Name	Class	Subclass	Filing Date If Appropriate
Α.						
EL	_ 5,821,796	10/13/1998	Yaklin, D., et al.	327	313	09/23/96
EL	_ 5,852,375	12/22/1998		327	108	02/07/97
EL	_ 5,877,061	03/02/1999		438	386	02/25/97
		FC	REIGN PATENT DOCUMENTS			
*Examiner	Document Number	Date	Country	Class	Subclass	Translation Yes No
Initial	_ 363066963A	03/01/1988	Japan	257	305	
	•	÷	OTHER DOCUMENTS			

**Examiner Initial	(Including Author, Title, Date, Pertinent Pages, Ecc.)
EL	Adler, E., et al., "The Evolution of IBM CMOS DRAM Technology", 167-188, (Jan./Mar., 1995)
EL	Asai, S., et al., "Technology Challenges for Integration Near and Below 0.1 micrometer", Proceedings of the IEEE, 85, Special Issue on Nanometer-Scale Science & Technology, 505-520, (Apr. 1997)
EL	Banerjee, S.K., et al., "Characterization of Trench Transistors for 3-D Memories", 1986 Symposium on VLSI Technology, Digest of Technical Papers, San Diego, CA, 79-80, (May 28-30, 1986)
EC	Blalock, T.N., et al., "A High-Speed Sensing Scheme for 1T Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier", IEEE Journal of Solid-State Circuits, 27(4), pp. 618-624, (April 1992)
CL	Bomchil, G., et al., "Porous Silicon: The Material and its Applications in Silicon-On-Insulator Technologies", Applied Surface Science, 41/42, 604-613, (1989)
EL	Burnett, D., et al., "Implications of Fundamental Threshold Voltage Variations for High-Density SRAM and Logic Circuits", 1994 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, HI, 15-16, (June 4-7, 1994)
GL	Burnett, D., et al., "Statistical Threshold-Voltage Variation and its Impact on Supply-Voltage Scaling", Proceedings SPIE: Microelectronic Device and Multilevel Interconnection Technology, 2636, 83-90, (1995)

		m Co
Examiner (Date Considered 4	8/03= -
*Substitute Disclosure Statement Form (PTO 1449)	is in conformance with MPEP 609; Draw line	through citation

if not in conformance and not considered. Another copy of this form with next communication to applicant.



Sheet 4 of 12

Form 1449*	Atty. Docket No.: 303.389US2	Scrial No. Unknown
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.	
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner Initial (Including Author, Title, Date, Pertinent Pages, Etc.)

er	Chen, M.J., et al., "Back-Gate Forward Bias Method for Low-Voltage CMOS Digital Cicuits", <u>IEEE Transactions on Electron Devices, 43</u> , 904-909, (June 1986)
CC	Chen, M.J., et al., "Optimizing the Match in Weakly Inverted MOSFET's by Gated Lateral Bipolar Action", <u>IEEE Transactions on Electron Devices</u> , 43, 766-773, (May 1996)
a	Chung, I.Y., et al., "A New SOI Inverter for Low Power Applications", <u>Proceedings of the 1996 IEEE International SOI Conference</u> , Sanibel Island, FL, 20-21, (Sep. 30-Oct. 3, 1996)
CL	De, V.K., et al., "Random MOSFET Parameter Fluctuation Limits to Gigascale Integration (GSI)", <u>1996 Symposium on VLSI Technology</u> , <u>Digest of Technical</u> <u>Papers</u> , Honolulu, HI, 198-199, (June 11-13, 1996)
a	Denton, J.P., et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", IEEE Electron Device Letters, 17(11), 509-511, (Nov. 1996)
64	Fong, Y., et al., "Oxides Grown on Textured Single-Crystal Silicon Dependence on Process and Application in EEPROMs", IEEE Transactions on Electron Devices, 37(3), pp. 583-590, (March 1990)
<u></u>	Forbes, L., et al., "Resonant Forward-Biased Guard-Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits", Electronics Letters, 31, 720-721, (April 1995)
EL	Foster, R., et al., "High Rate Low-Temperature Selective Tungsten", In: Tungsten and Other Refractory Metals for VLSI Applications III, V.A. Wells, ed., Materials Res. Soc., Pittsburgh, PA, 69-72, (1988)
- EL	Fuse, T., et al., "A 0.5V 200MHz 1-Stage 32b ALU Using a Body Bias Controlled SOI Pass-Gate Logic", 1997 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 286-287, (1997)
GL	Gong, S., et al., "Techniques for Reducing Switching Noise in High Speed Digital Systems", <u>Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit</u> , 21-24, (1995)

Examiner	Date Considered	41	18/03
*Substitute Disclosure Statement Form (ATO-1449)		- 1	•

^{**}EXAMINER: Initial if citation considered, thether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Sheet 5 of 12

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

a	Hao, M.Y., et al., "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon", <u>Appl. Phys. Lett.</u> , <u>60</u> , 445-447, (Jan. 1992)
V	Harada, M., et al., "Suppression of Threshold Voltage Variation in MTCMOS/SIMOX Circuit Operating Below 0.5 V", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 96-97, (June 11-13, 1996)
d	Heavens, O., Optical Properties of Thin Solid Films, Dover Pubs. Inc., New York, 167, (1965)
6C	Hisamoto, D., et al., "A New Stacked Cell Structure for Giga-Bit DRAMs using Vertical Ultra-Thin SOI (DELTA) MOSFETs", 1991 IEEE International Electron Devices Meeting, Technical Digest, Washington, D.C., 959-961, (Dec. 8-11, 1991)
	Hodges, D.A., et al., "MOS Decoders", <u>In: Analysis and Design of Digital</u> <u>Integrated Circuits, 2nd Edition</u> , Section: 9.1.3, 354-357, (1988)
el	Holman, W.T., et al., "A Compact Low Noise Operational Amplifier for a 1.2 Micrometer Digital CMOS Technology", IEEE Journal of Solid-State Circuits, 30, 710-714, (June 1995)
EL	Horie, H., et al., "Novel High Aspect Ratio Aluminum Plug for Logic/DRAM LSI's Using Polysilicon-Aluminum Substitute", <u>Technical Digest: IEEE</u> International Electron Devices Meeting, San Francisco, CA, 946-948, (1996)
ce	Hu, G., et al., "Will Flash Memory Replace Hard Disk Drive?", 1994 IEEE International Electron Device Meeting, Panel Discussion, Session 24, Outline, 1 p., (Dec. 13, 1994)
EL	Huang, W.L., et al., "TFSOI Complementary BiCMOS Technology for Low Power Applications", IEEE Transactions on Electron Devices, 42, 506-512, (Mar. 1995)
ci	Jun, Y.K., et al., "The Fabrication and Electrical Properties of Modulated Stacked Capacitor for Advanced DRAM Applications", IEEE Electron Device Letters, 13, 430-432, (Aug. 1992)

			$-\!$	/
Evaminer		Date Considered 4	IKI	<i>'</i> , _
Examiner	$c_1 \cdot / c_2 = c_1 \cdot c_2 \cdot c_2 \cdot c_3 \cdot c_4 \cdot c_4 \cdot c_4 \cdot c_5 \cdot c_5 \cdot c_5 \cdot c_6 \cdot c_$		101	<i>D</i> 3
		i		
			•	•

*Substitute Disclosure Statement Pope (PTO 1449)

^{**}EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Sheet 6 of 12

		
Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.	
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner Initial (Including Author, Title, Date, Pertinent Pages, Etc.)

c L	Jung, T.S., et al., "A 117-mm2 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications", <u>IEEE Journal of Solid-State Circuits</u> , 31, 1575-1582, (Nov. 1996)
V	Kang, H.K., et al., "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1Gbit DRAMs", <u>IEEE International Electron Devices Meeting</u> . Technical Digest, San Francisco, CA, 635-638, (Dec. 11-14, 1994)
EV	Kim, Y.S., et al., "A Study on Pyrolysis DMEAA for Selective Deposition of Aluminum", In: Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, R.C. Ellwanger, et al., (eds.), Materials Research Society, Pittsburgh, PA, 675-680, (1996)
er	Kishimoto, T., et al., "Well Structure by High-Energy Boron Implantation for Soft-Error Reduction in Dynamic Random Access Memories (DRAMs)", <u>Japanese</u> <u>Journal of Applied Physics</u> , 34, 6899-6902, (Dec. 1995)
66	Klaus, et al., "Atomic Layer Controlled Growth of SiO2 Films Using Binary Reaction Sequence Chemistry", <u>Applied Physics Lett. 70(9)</u> , 1092-94, (3 March 1997)
61	Kohyama, Y., et al., "Buried Bit-Line Cell for 64MB DRAMs", 1990 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, HI, 17-18, (June 4-7, 1990)
rel.	Koshida, N., et al., "Efficient Visible Photoluminescence from Porous Silicon", Japanese Journal of Applied Physics, 30, L1221- L1223, (July 1991)
60	Kuge, S., et al., "SOI-DRAM Circuit Technologies for Low Power High Speed Multigiga Scale Memories", IEEE Journal of Solid-State Circuits, 31(4), pp. 586-591, (April 1996)
40	Lantz, II, L., "Soft Errors Induced By Alpha Particles", <u>IEEE Transactions on</u> Reliability, 45, 174-179, (June 1996)
GL	Lehmann, et al., "A Novel Capacitor Technology Based on Porous Silicon", Thin Solid Films 276, Elsevier Science, 138-42, (1996)
EL	Lehmann, V., "The Physics of Macropore Formation in Low Doped n-Type Silicon", <u>Journal of the Electrochemical Society</u> , 140(10), 2836-2843, (Oct. 1993)

		\sim	 				
Examiner	2/	Tr	 Date 	Considered	41	8/	63

*Substitute Disclosure Statement Form 1770-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Form 1449*

Atty. Docket No.: 303.389US2

Serial No. Unknown

Applicant: Leonard Forbes et al.

BY APPLICANT
(Use several sheets if necessary)

Filing Date: Herewith

Group: Unknown

OTHER DOCUMENTS

**Examiner Initial (Including Author, Title, Date, Pertinent Pages, Etc.)

EL	Lu, N., et al., "The SPT Cell A New Substrate-Plate Trench Cell for DRAMs", 1985 IEEE International Electron Devices Meeting, Technical Digest, Washington, D.C., 771-772, (Dec. 1-4, 1985)
er	MacSweeney, D., et al., "Modelling of Lateral Bipolar Devices in a CMOS Process", <u>IEEE Bipolar Circuits and Technology Meeting</u> , Minneapolis, MN, 27-30, (Sep. 1996)
EC	Maeda, S., et al., "A Vertical Phi-Shape Transistor (VPhiT) Cell for 1 Gbit DRAM and Beyond", <u>1994 Symposium of VLSI Technology</u> , <u>Digest of Technical</u> <u>Papers</u> , Honolulu, HI, 133-134, (June 7-9, 1994)
64	Maeda, S., et al., "Impact of a Vertical Phi-Shape Transistor (VPhiT) Cell for 1 Gbit DRAM and Beyond", IEEE Transactions on Electron Devices, 42, 2117-2123, (Dec. 1995)
EL	Malaviya, S., <u>IBM TBD, 15</u> , p. 42, (July 1972)
GL	Masu, K., et al., "Multilevel Metallization Based on Al CVD", 1996 IEEE Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, HI, 44-45, (June 11-13, 1996)
66	McCredie, B.D., et al., "Modeling, Measurement, and Simulation of Simultaneous Switching Noise", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B, 19, 461-472, (Aug. 1996)
EL	Muller, K., et al., "Trench Storage Node Technology for Gigabit DRAM Generations", <u>Digest IEEE International Electron Devices Meeting</u> , San Francisco, CA, 507-510, (Dec. 1996)
EC	Nitayama, A., et al., "High Speed and Compact CMOS Circuits with Multipillar Surrounding Gate Transistors", IEEE Transactions on Electron Devices. 36, 2605-2606, (Nov. 1989)
60	Ohba, T., et al., "Evaluation on Selective Deposition of CVD W Films by Measurement of Surface Temperature", <u>In: Tungsten and Other Refractory Metals for VLSI Applications II</u> , Materials Research Society, Pittsburgh, PA, 59-66, (1987)

Examiner Date Considered 4/8/02			
7/10/07	Examiner 7	Date Considered	4/8/03

^{**}EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Sheet 8 of 12

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.	
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner Initial (Including Author, Title, Date, Pertinent Pages, Etc.)

a	Ohba, T., et al., "Selective Chemical Vapor Deposition of Tungsten Using Silane and Polysilane Reductions", <u>In: Tungsten and Other Refractory Metals for VLSI Applications IV</u> , Materials Research Society, Pittsburgh, PA, 17-25, (1989)
61	Ohno, Y., et al., "Estimation of the Charge Collection for the Soft-Error Immunity by the 3D-Device Simulation and the Quantitative Investigation", Simulation of Semiconductor Devices and Processes, 6, 302-305, (Sep. 1995)
GL	Oowaki, Y., et al., "New alpha-Particle Induced Soft Error Mechanism in a Three Dimensional Capacitor Cell", IEICE Transactions on Electronics, 78-C, 845-851, (July 1995)
ш	Oshida, S., et al., "Minority Carrier Collection in 256 M-bit DRAM Cell on Incidence of Alpha-Particle Analyzed by Three-Dimensional Device Simulation", IEICE Transactions on Electronics, 76-C, 1604-1610, (Nov. 1993)
el	Ott, A.W., et al., "Al3O3 Thin Film Growth on Si(100) Using Binary Reaction Sequence Chemistry", Thin Solid Films, Vol. 292, 135-44, (1997)
EL	Ozaki, T., et al., "A Surrounding Isolation-Merged Plate Electrode (SIMPLE) Cell with Checkered Layout for 256Mbit DRAMs and Beyond", 1991 IEEE International Electron Devices Meeting, Washington, D.C., 469-472, (Dec. 8-11, 1991)
W	Parke, S.A., et al., "A High-Performance Lateral Bipolar Transistor Fabricated on SIMOX", <u>IEEE Electron Device Letters</u> , 14, 33-35, (Jan. 1993)
	Pein, H., et al., "A 3-D Sidewall Flash EPROM Cell and Memory Array", IEEE Transactions on Electron Devices, 40, 2126-2127, (Nov. 1993)
86	Pein, H., et al., "Performance of the 3-D PENCIL Flash EPROM Cell and Memory Array", IEEE Transactions on Electron Devices, 42, 1982-1991, (November, 1995)
Ol	Pein, H.B., et al., "Performance of the 3-D Sidewall Flash EPROM Cell", IEEE International Electron Devices Meeting, Technical Digest, 11-14, (1993)
EL	Ramo, S., et al., "Fields and Waves in Communication Electronics", John Wiley & Sons, Inc., New York, 3rd ed., 428-433, (1994)

			<u> </u>
Examiner 9	Date Considered 9	8/	03
*Substitute Disclosure Statement Form (PTO-14-9)			

-- EXAMINER. Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

.



Sheet 9 of 12

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown	
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.		
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown	

OTHER DOCUMENTS

**Examiner (Including Author, Title, Date, Pertinent Pages, Ecc.)
Initial

EL	Rao, K.V., et al., "Trench Capacitor Design Issues in VLSI DRAM Cells", <u>1986</u> <u>IEEE International Electron Devices Meeting, Technical Digest</u> , Los Angeles, CA, 140-143, (Dec. 7-10, 1986)
60	Richardson, W.F., et al., "A Trench Transistor Cross-Point DRAM Cell", IEEE International Electron Devices Meeting, Washington, D.C., 714-717, (Dec. 1-4, 1985)
U	Sagara, K., et al., "A 0.72 micro-meter2 Recessed STC (RSTC) Technology for 256Mbit DRAMs using Quarter-Micron Phase-Shift Lithography", 1992 Symposium on VLSI Technology, Digest of Technical Papers, Seattle, WA, 10-11, (June 2-4, 1992)
EC	Saito, M., et al., "Technique for Controlling Effective Vth in Multi-Gbit DRAM Sense Amplifier", <u>1996 Symposium on VLSI Circuits</u> , <u>Digest of Technical</u> <u>Papers</u> , Honolulu, HI, 106-107, (June 13-15, 1996)
6L	Senthinathan, R., et al., "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers", IEEE Transactions on Microwave Theory and Techniques, 42, 1765-1773, (Sep. 1994)
CL	Shah, A.H., et al., "A 4-Mbit DRAM with Trench-Transistor Cell", IEEE Journal of Solid-State Circuits, SC-21, 618-625, (Oct. 1986)
er	Shah, A.H., et al., "A 4Mb DRAM with Cross-Point Trench Transistor Cell", 1986 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 268-269, (Feb. 21, 1986)
a	Sherony, M.J., et al., "Reduction of Threshold Voltage Sensitivity in SOI MOSFET's", IEEE Electron Device Letters, 16, 100-102, (Mar. 1995)
a	Shimomura, K., et al., "A 1V 46ns 16Mb SOI-DRAM with Body Control Technique", 1997 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 68-69, (Feb. 6, 1997)
cs	Stanisic, B.R., et al., "Addressing Noise Decoupling in Mixed-Signal IC's: Power Distribution Design and Cell Customization", IEEE Journal of Solid-State Circuits, 30, 321-326, (Mar. 1995)

Examiner A	Date Considered	4/8/07
1000 1440)		

*Substitute Disclosure Scatement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPRP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

..

•



Sheet 10 of 12

Form 1449*	Atty. Docket No.: 303.389US2 Serial No. Unknown		
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.		
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown	

OTHER DOCUMENTS

	OTHER DOCUMENTS
**Examiner	(Including Author, Title, Date, Pertinent Pages, Etc.)
Initial	

EL	Stellwag, T.B., et al., "A Vertically-Integrated GaAs Bipolar DRAM Cell", IEEE Transactions on Electron Devices, 38, 2704-2705, (Dec. 1991)
60	Suma, K., et al., "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology", IEEE Journal of Solid-State Circuits, 29(11), pp. 1323-1329, (November 1994)
EL	Sunouchi, K., et al., "A Surrounding Gate Transistor (SGT) Cell for 64/256Mbit DRAMs", 1989 IEEE International Electron Devices Meeting, Technical Digest, Washington, D.C., 23-26, (Dec. 3-6, 1989)
ev	Sunouchi, K., et al., "Process Integration for 64M DRAM Using an Asymmetrical Stacked Trench Capacitor (AST) Cell", 1990 IEEE International Electron Devices Meeting, San Francisco, CA, 647-650, (Dec. 9-12, 1990)
eV	Suntola, T., "Atomic Layer Epitaxy", Handbook of Crystal Growth 3, Thin Films of Epitaxy, Part B: Growth Mechanics and Dynamics, Elsevier, Amsterdam, 601-63, (1994)
W	Sze, S.M., <u>VLSI Technology</u> , 2nd Edition, Mc Graw-Hill, NY, 90, (1988)
w	Takai, M., et al., "Direct Measurement and Improvement of Local Soft Error Susceptibility in Dynamic Random Access Memories", Nuclear Instruments & Methods in Physics Research, B-99, Proceedings of the 13th International Conference on the Application of Accelerators in Research and Industry, Denton, TX, 562-565, (Nov. 7-10, 1994)
6C	Takato, H., et al., "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEEE International Electron Devices Meeting, Technical Digest, 222-225, (1988)
60	Takato, H., et al., "Impact of Surrounding Gate Transistor (SGT) for Ultra-High Density LSI's", <u>IEEE Transactions on Electron Devices</u> , 38, 573-578, (Mar. 1991)
cl	Tanabe, N.; et al., "A Ferroelectric Capacitor Over Bit-Line (F-COB) Cell for High Density Nonvolatile Ferroelectric Memories", 1995 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, Japan, 123-124, (June 6-8, 1995)

Examiner	90	1	Date Considered	4/	8/03
*Substitute Disclosu	re Statement Form (PTO-	14457			·

**EXAMINER: Initial if citation considered whether or not citation is in conformance with MPEF 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

.....



Sheet 11 of 12

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.	
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

OTHER DOCUMENTS					
•• Examiner	(Including Author, Title, Date, Pertinent Pages, Etc.)				
Initial					

61	Temmler, D., "Multilayer Vertical Stacked Capacitors (MVSTC) for 64Mbit and 256Mbit DRAMs", 1991 Symposium on VLSI Technology, Digest of Technical Papers, Oiso, 13-14, (May 28-30, 1991)
cL	Terauchi, M., et al., "A Surrounding Gate Transistor (SGT) Gain Cell for Ultra High Density DRAMs", <u>1993 Symposium on VLSI Technology, Digest of Technical Papers</u> , Kyoto, Japan, 21-22, (1993)
CL	Tsui, P.G., et al., "A Versatile Half-Micron Complementary BiCMOS Technology for Microprocessor-Based Smart Power Applications", <u>IEEE Transactions on Electron Devices</u> , 42, 564-570, (Mar. 1995)
CL	Verdonckt-Vandebroek, S., et al., "High-Gain Lateral Bipolar Action in a MOSFET Structure", <u>IEEE Transactions on Electron Devices 38</u> , 2487-2496, (Nov. 1991)
	Vittal, A., et al., "Clock Skew Optimization for Ground Bounce Control", 1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, San Jose, CA, 395-399, (Nov. 10-14, 1996)
EL	Wang, N., <u>Digital MOS Integrated Circuits</u> , Prentice Hall, Inc., Englewood Cliffs, NJ, p. 328-333, (1989)
EL	Wang, P.W., et al., "Excellent Emission Characteristics of Tunneling Oxides Formed Using Ultrathin Silicon Films for Flash Memory Devices", <u>Japanese</u> <u>Journal of Applied Physics</u> , 35, 3369-3373, (June 1996)
d	Watanabe, H., et al., "A New Cylindrical Capacitor Using Hemispherical Grained Si (HSG-Si) for 256Mb DRAMs", IEEE International Electron Devices Meeting, Technical Digest, San Francisco, CA, 259-262, (Dec. 13-16, 1992)
EL	Watanabe, H., et al., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", <u>1993 Symposium on VLSI Technology</u> , <u>Digest of</u> <u>Technical Papers</u> , Kyoto, Japan, 17-18, (1993)
el	Watanabe, H., et al., "An Advanced Fabrication Technology of Hemispherical Grained (HSG) Poly-Si for High Capacitance Storage Electrodes", Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, Japan, 478-480, (1991)

Examiner	nn	Date Considered	4/8/03

^{*}Substitute Disclosure Statement Form (PTO 1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609: Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Sheet 12 of 12

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT	Applicant: Leonard Forbes et al.	
BY APPLICANT (Use several sheets if necessary)	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

Olithic Docomming				
**Examiner	(including Author, Title, Date, Pertinent Pages, Scc.)			
Initial				

EL	Watanabe, H., et al., "Device Application and Structure Observation for Hemispherical-Grained Si", J. Appl. Phys., 71, 3538-3543, (Apr. 1992)
eL	Watanabe, H., et al., "Hemispherical Grained Silicon (HSG-Si) Formation on In-Situ Phosphorous Doped Amorphous-Si Using the Seeding Method", Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, Japan, 422-424, (1992)
el	Watanabe, S., et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", <u>IEEE Journal of</u> Solid-State Circuits, 30, 960-971, (Sep. 1995)
6V	Wooley, et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", IEEE Journal of Solid State Circuits, Vol SC-28, 420-30, (1993)
66	Yamada, T., et al., "A New Cell Structure with a Spread Source/Drain (SSD) MOSFET and a Cylindrical Capacitor for 64-Mb DRAM's", IEEE Transactions on Electron Devices, 38, 2481-2486, (Nov. 1991)
EL	Yamada, T., et al., "Spread Source/Drain (SSD) MOSFET Using Selective Silicon Growth for 64Mbit DRAMs", 1989 IEEE International Electron Devices Meeting, Technical Digest, Washington, D.C., 35-38, (Dec. 3-6, 1989)
66	Yoshikawa, K., "Impact of Cell Threshold Voltage Distribution in the Array of Flash Memories on Scaled and Multilevel Flash Cell Design", 1996 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, HI, 240-241, (June 11-13, 1996)

Examiner	9-2-1	2	Date Considered	4/8/0	<u>_3</u>

*Substitute Disclosure Statement Form (PTO-1449)

^{**}EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. The lade copy of this form with next communication to applicant.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) FEB 0 3 2003 Sheet 1 of 1

Application Number	09/467992	
Filing Date	December 20, 1999	
First Named Inventor	Forbes, Leonard	
Group Art Unit	2815	
Examiner Name	Lee, Eugene	

US PATENT DOCUMENTS						
Examiner USP Document Publication Date Initial Number			Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
61/	US-6,238,976	05/29/2001	Noble, W. P., et al	438	259	02/27/1998

	FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²

1		OTHER	OCUMENTS NON PATENT LITERATURE DOCUMENTS		
	Examiner	Cite	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item	T ²	
	Initials*	No ¹	(book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s),	1	
			publisher, city and/or country where published.	i	

TECHNOLOGY CENTER 2800

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to number (optional) 2 Applicant is to place a check mark here if English language Translation is attached · EXAMINER: Initial if reference considered, whether or not citation is in conforman applicant.1 Applicant's unique citation designati